ABSTRACT OF THE DISCLOSURE

A non-volatile semiconductor memory device is disclosed, which comprises a memory cell unit including at least one memory cell transistor formed on a semiconductor substrate and having a laminated structure of a charge accumulation layer and a control gate layer, and a selection gate transistor one of the source/drain diffusion layer regions of which is connected to a bit line or a source line and the other of the the source/drain diffusion layer regions of which is connected to the memory cell unit. The shape of the source diffusion layer region of the selection gate transistor is asymmetical to the shape of the drain diffusion layer region thereof below the selection gate transistor.